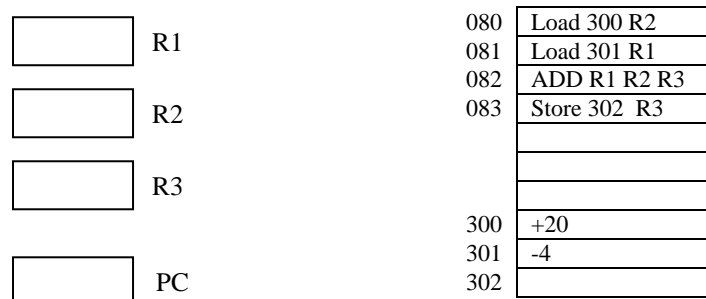**A**

True/ False

1	Registers are fast stand-alone storage location that hold data temporarily.	
2	The instruction Register keeps track of the instructions currently being executed.	
3	There are three design for CPU architectures: CISC, RISC, and SCSI	
4	The contents of storage devices are volatile	
5	A magnetic tape is considered a sequential access device	
6	The number of wires of Data Bus depends on the address space of the memory	
7	A job is a nonactive set of instructions stored in disk	
8	The programing in RISC is more difficult and longer than CISC	
9	Partioning is asituation in which a process is unable to execute due to unrestricted use of resources by other processes	
10	An Example of RISC architecture is the Pentium series of processors developed by Intel	
11	An Operating System is a hardware that manages all the computer resources	
12	Time sharing means the Resources can be shared between different jobs	
13	In paging system, if the page size is 4 MB and we have a progarm needs 17 MB, so this progarm will use 4 pages.	
14	The SRAM is faster than DRAM	
15	Each process is a program	
16	Starvation occurs when the operating system does not put resource restriction on processes	
17	UNIX is a portable operating system	
18	The device manager controls access to files.	
19	When the job moves to the ready state it becoms a process.	
20	To run an instruction in a program, the control unit first fetches the instruction, decodes it, and then executes it.	

Multiple Choice

21. …………. Is a memory type with capacitors that need to be refreshed periodically
  - a. SRAM
  - b. ROM
  - c. PROM
  - d. None of the above

22. …………. Can be programmed and erased using electronic impulses but can be remain in a computer during erasure
  - a ROM
  - b. EEPROM
  - c. EPROM
  - d. PROM

	R1
	R2
	R3
	PC

080	Load 300 R2
081	Load 301 R1
082	ADD R1 R2 R3
083	Store 302 R3
300	+20
301	-4
302	

Using this figure, answer the following questions (23 – 27)

23. In the beginning the PC will contain
  - a. 300
  - b. +20
  - c. 080
  - d. -4

24. After the first operation, The R1 will contain
  - a. +20
  - b. 300
  - c. -4
  - d. Nothing

25. After the second operation The R2 will contain
  - a. +20
  - b. 300
  - c. -4
  - d. Nothing

26. After the third operation The R3 will contain
  - a. 24
  - b. -16
  - c. 16
  - d. nothing

27. After the fourth operation The PC will contain
  - a. 303
  - c. 083

b. 302   d. 084

28. CPU registers should have …… speed memory.
   - a. High
   - b. low
   - c. medium
   - d. none of the above

29. there are …….. bytes in 8 mega bytes (8MB)
   - a. 2^{21}
   - b. 2^{22}
   - c. 2^{23}
   - d. 2^{24}

30. A system with more than one CPU requires …………. Operating system.
   - a. Batch
   - b. Time-sharing
   - c. distributed
   - d. parallel

31. …………. is multiprogramming with swapping
   - a. Partioning
   - b. Demand paging
   - c. Paging
   - d. Queuing

32. In …………. , many program can reside in memory.
   - a. Time-sharing
   - b. monoprogramming
   - c. Multiprogramming
   - d. Parallel processing

33. In paging, a memory is divided into equally sized sections called ………..
   - a. frames
   - b. Pages
   - c. segments
   - d. partions

34. A process in the …….. state can go to either the ready, terminated, or waiting state.
   - a. Hold
   - b. Runing
   - c. virtual
   - d. a and b

35. A computer has 256 MB of memory. Each word in this computer is 32 bytes. How many bits are needed to address any single word in memory ?
   - a. 22
   - b. 23
   - c. 24
   - d. 25

36. The …… manager is resbonsible for access to I/O
   - a. memory
   - b. Device
   - c. process
   - d. file

37. A …. is a program that is selected for execution
   - a. Process
   - b. Code
   - c. Task
   - d. Job

38. A …. is a job residing in memory
   - a. Process
   - b. Code
   - c. Task
   - d. Job

39. ……….. …… wait in queues.
   - a. Jobs and programs
   - b. Jobs and tasks
   - c. Jobs and processes
   - d. Tasks and processes

40. In demand segmentation, the program can be divided into ……….. sized sections
   - a. Equal
   - b. Different
   - c. a and b
   - d. none of the above